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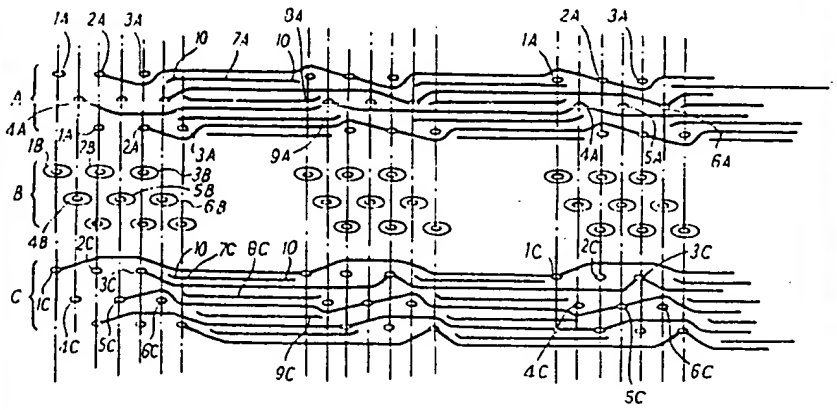
(54) Multilayer Printed Circuit Board

(57) A printed circuit board comprises upper and lower layers (A, C) having terminals (1A—6A), (1C—6C) for connection to pins of electrical connectors or electronic components which are to be connected in parallel be conductor tracks of the circuit board. In order to achieve an even distribution of conductor tracks between the layers (A, C) the terminals (2A, 4A, 6A), (1C, 3C, 5C) are connected to conductor tracks, the terminals(1A, 3A, 5A,), (2C, 4C, 6C) are unconnected to conductor tracks, and terminals (1A, 3A, 5A) and (2A, 4A, 6A) are connected through the board to terminals (1C, 3C, 5C) and (2C, 4C, 6C) respectively. A conductive layer (B) providing a ground plane may be located between the upper and lower layers (A, C) and has non-conductive areas (1B—6B) providing clearance for plated-through holes, which may provide connection between tracks A and C.

Tracks (7A—9A), (7C—9C), located between the conductor tracks, may be connected to the ground plane (B) by plated-through holes (10) so that they form closed conductive loops providing shielding against capacitative and inductive cross-talk between the conductor tracks.

FIG. 4



The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

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SPECIFICATION
Printed Circuit Board

This invention concerns improvements in printed circuit boards, and relates more especially to printed circuit boards of the kind bearing multiple conductor arrays such as may form data buses of a data processor, e.g. a microprocessor.

With the increasing miniaturisation of data processors there is a corresponding demand for printed circuit boards in which the area occupied by a given number of conductor tracks is reduced to a minimum. In the case of conductor arrays such as form data buses, and thus comprise a simple array of parallel conductor tracks, the number of tracks capable of being accommodated in a given area is theoretically limited only by the minimum width of conductive track giving acceptable resistance of the conductor and the minimum distance between adjacent tracks necessary to achieve acceptable isolation of the respective conductors. In practice, however, the termination of the conductor tracks at individual electronic components or electrical terminal connectors imposes limits upon the physical spacing of the conductors. Also, with high frequency and square wave signals such as occur in microprocessor systems, cross-talk between conductors increases significantly as the distance between conductors is reduced. Mitigation of these problems is therefore highly desirable in order to achieve improved standards of miniaturisation.

In accordance with one aspect of the invention there is provided a printed circuit board comprising an array of parallel conductor tracks spaced apart from one another, on one side of the board; an array of parallel conductive shielding tracks arranged on said one side of the board between said conductor tracks such that adjacent pairs of conductor tracks are each separated by an intermediate shielding track; conductor means provided on a further side of the board; and means electrically connecting each of said shielding tracks at points spaced along its length to the, or a corresponding, conductor means on said further side of the printed circuit board, whereby each said shielding track, in combination with the, or the corresponding, conductor means on said further side of the board forms one or more closed, electrically conductive loops.

In an arrangement according to this aspect of the invention the said shielding tracks perform a twofold, and thus highly effective, shielding function in relation to said array of conductive tracks. Firstly, the physical location of the shielding tracks between the conductors, provides, more effectively when the shielding tracks are suitably connected to earth, shielding against capacitative cross-talk. Secondly, the connection of the shield tracks as closed loops in a plane at 90° to the plane of the board, provides shielding against inductive cross-talk, since electromagnetic fields due to signals in the electrical conductors set up eddy currents in, and are thus absorbed by, the said closed loops.

Preferably, the said conductor means on the said further layer or side of the printed circuit board comprises a ground plane provided by a continuous area of conductive material, and the said shielding conductors are electrically connected to said ground plane by means of so-called "plated-through holes". Plated-through holes are a means, well known in the art of printed circuit boards, for providing an electrical connection between conductor tracks between the respective layers of multiple sided printed circuit boards.

Although an arrangement in accordance with the invention provides for substantially reduced cross-talk between adjacent parallel conductor tracks, the requirement for additional shielding tracks intermediate to the conductor tracks does, to some extent reduce the number of conductor tracks capable of being accommodated within a given area. The correspondingly reduced density of the conductor tracks may be compensated for by providing two sets of conductor tracks on opposite sides of a printed circuit board, and arranging such tracks so that they connect with terminal locations common to both sides of the board.

According to another aspect of the invention, therefore, there is provided a printed circuit board including at least two layers, each of which comprises an array of parallel conductor tracks spaced apart from one another, and one or more arrays of terminal locations common to both layers of the board, said terminal locations of each array being arranged in rows extending transversely of the longitudinal axes of the said conductor track, and each said array including at least two such rows spaced apart in the direction of the longitudinal axes of said conductor tracks, the number of said terminal locations being equal to the total number of conductor tracks of both said layers, a substantially equal number of said conductor tracks of each layer connecting with respective ones of said terminal locations, the remaining terminal locations being connected to tracks of that layer, and the terminal locations of both layers of the board being interconnected by electrically conducting means extending between the respective layers of the board. Preferably, the said electrically conductive means comprise "plated-through holes".

According to a particularly advantageous embodiment of the invention, a conductor arrangement as defined above may be applied to a so-called "Eurocard" arrangement which comprises a 64 or 96-way DIN standard terminal connector, of which the 96 terminals are arranged in two or three rows respectively, each row containing 32 terminal locations at a spacing of 0.1". By utilising a double-sided printed circuit board having correspondingly located terminal positions, it has proved possible in accordance with the invention to provide all 96 conductor tracks connecting to the 96 terminal positions of the DIN connector, the conductor tracks being

equally distributed between the two sides of the printed circuit board and having shielding tracks arranged in alternation therewith. Such an arrangement provides maximum utilisation of the two surfaces of the board of the electrical conductors, and the location thereof within the area dictated by the standard terminal connections. Preferably the board is a three-layer board in which an electrically conductive ground plane is interposed between the two surfaces of the board bearing the conductor arrays. The ground plane is connected to the shielding conductors, by means of plated-through holes as described above, and the conductive area of the ground plane includes clearance holes enabling the plated-through connection of the conductor arrays and the terminal locations, with electrical isolation from the ground plane.

This invention is illustrated by way of example in the accompanying drawings, in which:

Fig. 1 is a plan view (actual size) showing the conductor and terminal arrangement of one layer of a typical three-layer printed circuit board in accordance with the invention, viewed from the component side of the board, in this figure only 84 "bussed" tracks were chosen in order to provide increased current carrying capacity on the outer rows of the connector,

Fig. 2 is a plan view showing the arrangement of the conductive layer of a second layer of the printed circuit board, providing a ground plane,

Fig. 3 is a plan view, similar to Fig. 1, showing the conductor and terminal arrangement of the third layer of the printed circuit board, viewed from the solder-side of the board, i.e. viewed from the opposite side of the board from that of the view shown in Fig. 1, and

Fig. 4 is a diagrammatic perspective view illustrating the relationship between the respective conductor arrangements of the layers of Figs. 1 to 3, over a small fragment of the area of the printed circuit board.

Referring to Figs. 1 to 3 of the drawings, it will be seen that the conductor arrangements shown therein comprise, at least in the case of Figs. 1 and 3, a repetitive pattern extending transversely and lengthwise of the printed circuit board. In the case of the ground plane of Fig. 2, the conductive layers of the board provides a continuous conductive area which is interrupted only by clearance holes providing for electrical connection between the conductors of the layers of Figs. 1 and 3. The complete printed circuit board comprises the conductive layers of Figs. 1 and 3 arranged in back-to-back relationship, with the conductive pattern of Fig. 2 arranged as an intermediate ground plane sandwiched therebetween. The terminal locations indicated at 1 in Figs. 1 and 3 are located in register with one another and interconnected by plated-through holes which pass through non-conductive areas 2 of the ground plane, and further plated-through holes indicated at 3 in Figs. 1 and 3 provide electrical connection between shielding tracks of Figs. 1 and 2, and the conductive area of the ground plane of Figs. 2, as will be described in more detail below.

Referring to Fig. 4, the relationship between the respective conductive patterns of the layers of Figs. 1 to 3 is illustrated in more detail, wherein a small fragment of the repetitive pattern of the respective layers is shown in an exploded perspective diagrammatic view. In Fig. 4, the area A represents a fragment of the pattern shown in Fig. 1 the area B represents a fragment of the pattern shown in Fig. 2, and the area C represents a fragment of the pattern shown in Fig. 3. The left-hand edge of the drawing illustrates the conductor pattern at a terminal edge of the printed circuit board, whereas the conductor pattern extending towards the right-hand edge of the drawing is repeated continuously until it terminates in an edge pattern (not shown), in symmetry with that at the left-hand edge of the drawing. The pattern is also repeated in the transverse direction, as can be seen by reference to Figs. 1 to 3. Each end of the tracking arrangement may alternatively be terminated by an electrical network which forms a termination impedance matched to the characteristic impedance of the tracks when considered as transmission lines.

The conductor tracks of the upper and lower layers of the printed circuit board shown in Figs. 1 and 3 respectively effectively connect in parallel a plurality of terminal locations which may be a sub-divided into groups of six as illustrated in Fig. 4 at 1A to 6A and 1C to 6C for the upper and lower layers respectively. The conductors of the upper tracks are directly connected to terminal locations 2A, 4A and 6A respectively, whereas those of the lower tracks are connected to locations 1C, 3C and 5C respectively. The unconnected locations 1A, 3A and 5A of the upper side are electrically connected by plated-through holes to location 1C, 3C and 5C of the lower track, whereas the corresponding unconnected areas 2C, 4C and 6C of the lower track are likewise connected to the areas 2A, 4A and 6A of the upper track. Thus of each group of six terminals of a terminal connector secured to the printed circuit board, three are connected to conductor tracks of the upper layers and three to conductor tracks of the lower layers, so that the conductor tracks connected to the terminal of the connector are evenly distributed between the upper and lower layers of the printed circuit board. This fact in itself would aid the minimisation of cross-talk between adjacent conductors because the spacing between such conductors is maximised, indeed it is only because the spacing has been maximised in this way, it is physically possible to interpose shielding tracks between conducting tracks on a backplane using the DIN 41612 connector leaving sufficient space to achieve acceptable isolation between all tracks.

As mentioned above, between the upper and lower layers of the printed circuit board which provide the arrays of conductor tracks, there is

interposed a ground plane of which the conductive pattern is illustrated at B in Fig. 4. The ground plane comprises a continuous layer of electrically conductive material which is broken only by non-conductive areas 1B to 6B at the centre of which are located apertures registering with the terminal areas 1A to 6A and 1C to 6C and accommodating the plated-through electrical connection between the upper and lower layers. The non-electrically conductive areas 1B to 6B are provided solely in order to avoid any unintentional electrical connection between the upper and lower terminal locations 1A to 6A, 1C to 6C and the electrically conductive layer of the ground plane.

Between each adjacent pair of electrically conductive tracks of the upper and lower layers A and C, there is arranged a shielding track indicated in Fig. 4 at 7A, 8A and 9A and 7C, 8C and 9C, respectively. Adjacent to each end of the shielding tracks 7A, 8A and 9A and 7C, 8C and 9C are arranged apertures 10 penetrating the printed circuit board, which apertures provide for plated-through connections between the corresponding point on the shielding tracks and the electrically conductive layer of the ground plane. Thus, each of the shield tracks 7A to 9A, 7C to 9C, in conjunction with the conductive layer of the ground plane B forms a closed-electrically conductive loop. Thus, electrically conductive shield tracks provide both capacitative shielding between adjacent conductive tracks, especially due to their electrical connection, via the ground plane, to earth, and inductive shielding of adjacent conductive tracks, due to the fact that eddy currents are induced therein by the electromagnetic fields set up by signal currents in the said conductor tracks. The said electromagnetic fields are thus absorbed within the electrically conductive loops provided by the shield tracks and inductive cross-talk between adjacent conductive tracks is correspondingly reduced.

From the above disclosure it will be appreciated that there has been provided a novel printed circuit board arrangement which provides optimum utilisation of the available printed circuit board area both as regards the density of distribution of the conductor tracks and as regards the utilisation of the intermediate shielding tracks to counteract cross-talk.

It will be appreciated that various alterations and modifications to the preferred embodiment of the invention described above may be made without departing from the scope of the invention as defined in the appended Claims. In particular, although the distribution of conductor tracks between upper and lower surfaces of the printed circuit board provides for optimum distribution of the conductor tracks, this may be dispensed with in cases where the required density of conductor distribution can be provided by a single conductive layer, and the reduction of cross-talk by means of the intermediate shielding track is of greater importance. In cases where the distribution of conductor tracks between the upper and lower layers, in order to achieve optimum spacing of the conductor tracks is of greater importance, such an arrangement may be utilised without the necessity for intermediate shielding tracks.

In addition the connection of each terminal on the connector to the corresponding terminal on all other connectors may be made on either side of the printed circuit board, or even, alternately on one side then on the other side between all the connectors on the printed circuit board. One further possible tracking arrangement exists which could have particular advantages in certain circumstances: the connection of tracks between all connectors along the printed circuit board could be made alternatively on one side, then the other between all the connectors such that an effective spiral of two or more conducting tracks takes place along the printed circuit board, this arrangement provides a "twisted pair" like transmission line down the length of the printed circuit board. The twist being provided by the effective crossing over of conducting tracks at or near each plated-through hole.

Claims

1. A printed circuit board comprising an array of parallel conductor tracks spaced apart from one another, on one side of the board; an array of parallel conductive shielding tracks arranged on said one side of the board between said conductor tracks such that adjacent pairs of conductor tracks are each separated by an intermediate shielding track; conductor means electrically connecting each of said shielding tracks at points spaced along its length to the, or a corresponding, conductor means on said further side of the printed circuit board, whereby each said shielding track, in combination with the, or the corresponding conductor means on said further side of the board forms one or more closed, electrically conductive loops.

2. A circuit board as claimed in Claim 1, wherein the said conductor means on the said further side of the printed circuit board comprises a ground plane provided by a continuous area of conductive material, and the said shielding conductors are electrically connected to said ground plane by means of so-called "plated-through holes".

3. A circuit board as claimed in Claim 1 or 2, including at least two layers each of which comprises an array of parallel conductor tracks spaced apart from one another, and one or more arrays of terminal locations common to both layers of the board, said terminal locations of each array being arranged in row extending transversely of the longitudinal axes of the said conductor track, and each said array including at least two such rows spaced apart in the direction of the longitudinal axes of said conductor tracks, the number of said terminal locations being equal to the total number of conductor tracks of both said layers, a substantially equal number of said

conductor tracks of each layer connecting with respective ones of said terminal locations, the remaining terminal locations being unconnected to tracks of that layer, and the terminal locations of both layers of the board being interconnected by electrically conducting means extending between the respective layers of the board.

4. A printed circuit board including at least two layers each of which comprises an array of parallel conductor tracks spaced apart from one another, and one or more arrays of terminal locations common to both layers of the board, said terminal locations of each array being arranged in rows extending transversely of the longitudinal axes of the said conductor track, and each array including at least two such rows spaced apart in the direction of the longitudinal axes of said conductor tracks, the number of said terminal locations being equal to the total number of conductor tracks of both said layers, a substantially equal number of said conductor tracks of each layer connecting with respective ones of said terminal locations, the remaining terminal locations being unconnected to tracks of that layer, and the terminal locations of both layers of the board being interconnected by electrically conducting means extending between the respective layers of the board.

5. A printed circuit board as claimed in any one of Claims 1—4, including at least two layers each of which comprises a plurality of arrays of parallel conductor tracks mutually spaced in the direction of their longitudinal axes, longitudinally and laterally adjacent conductor tracks on different layers of the board being electrically connected together to form composite conductors extending longitudinally of the circuit board and including conductor tracks from different layers arranged in alternation and helically connected, laterally adjacent ones of said composite conductors being mutually entwined in the manner of a twisted pair.

6. A printed circuit board including at least two layers each of which comprises a plurality of arrays of parallel conductor tracks mutually spaced in the direction of their longitudinal axes, longitudinally and laterally adjacent conductor tracks on different layers of the board being electrically connected together to form composite conductors extending longitudinally of the circuit board and including conductor tracks from different layers arranged in alternation and helically connected, laterally adjacent ones of said composite conductors being mutually entwined in the manner of a twisted pair.

7. A printed circuit board substantially as described herein with reference to the accompanying drawings.

8. The features as herein described, or their equivalents, in any novel selection.

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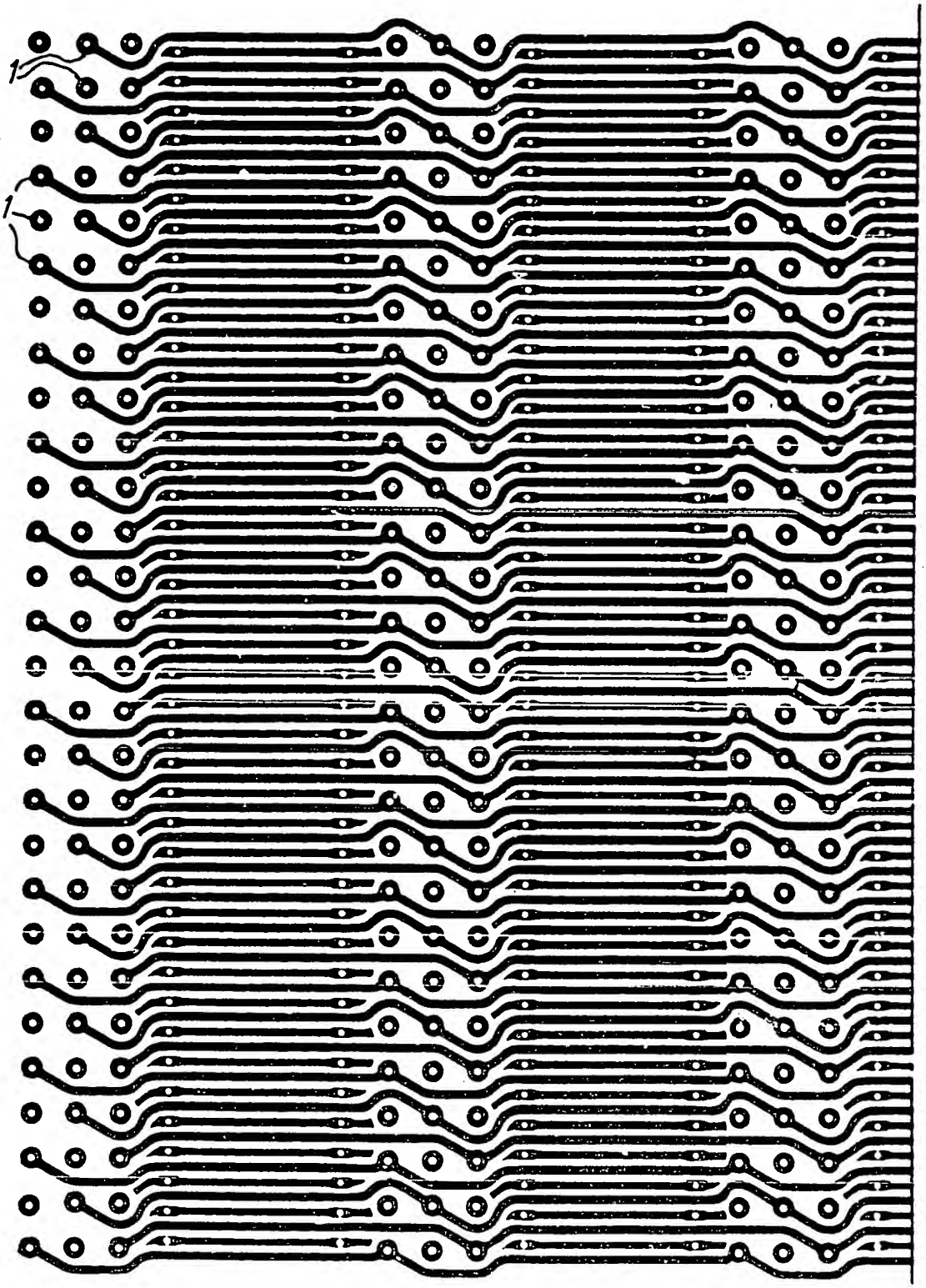
FIG. 1



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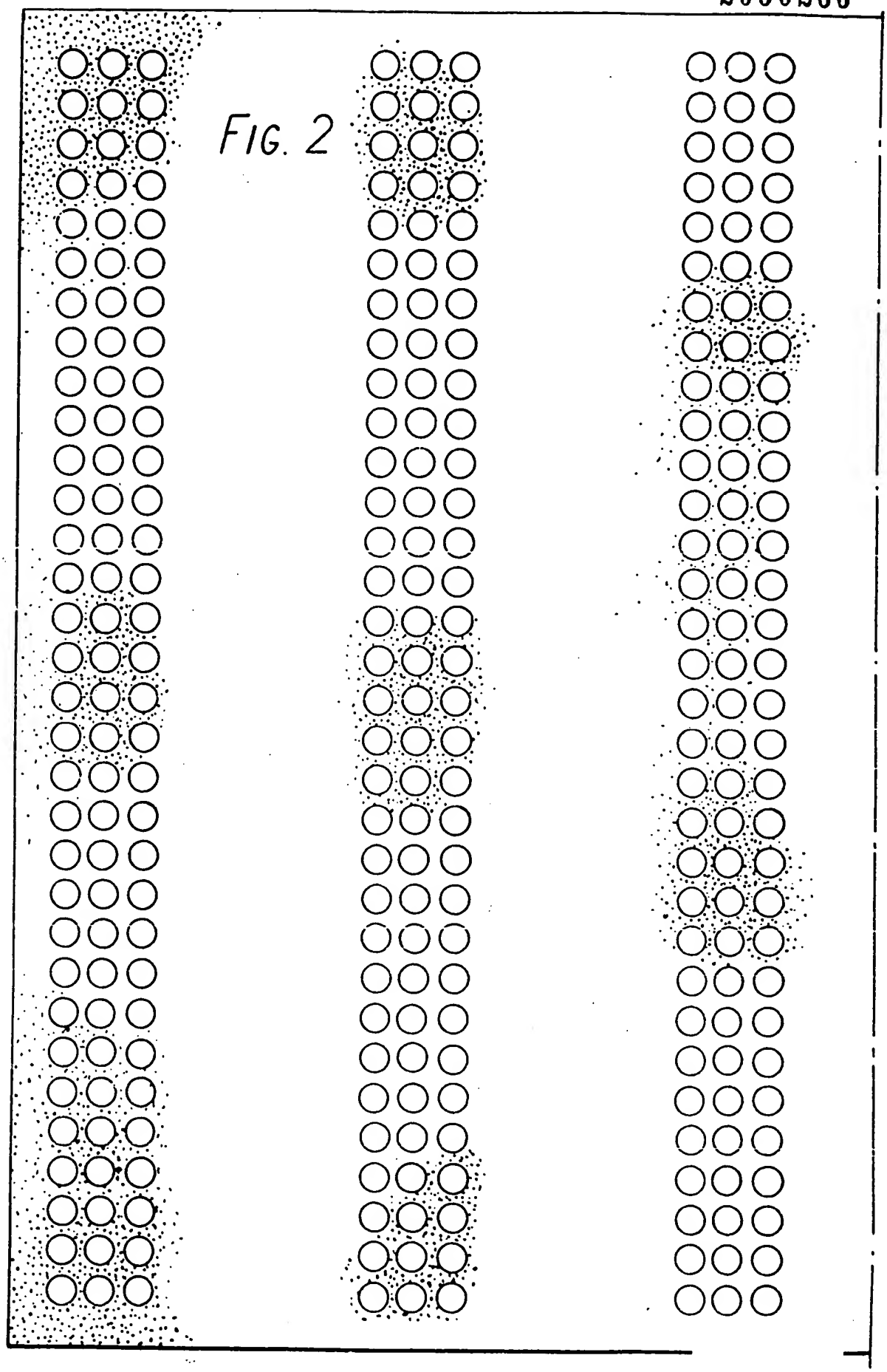

FIG. 2

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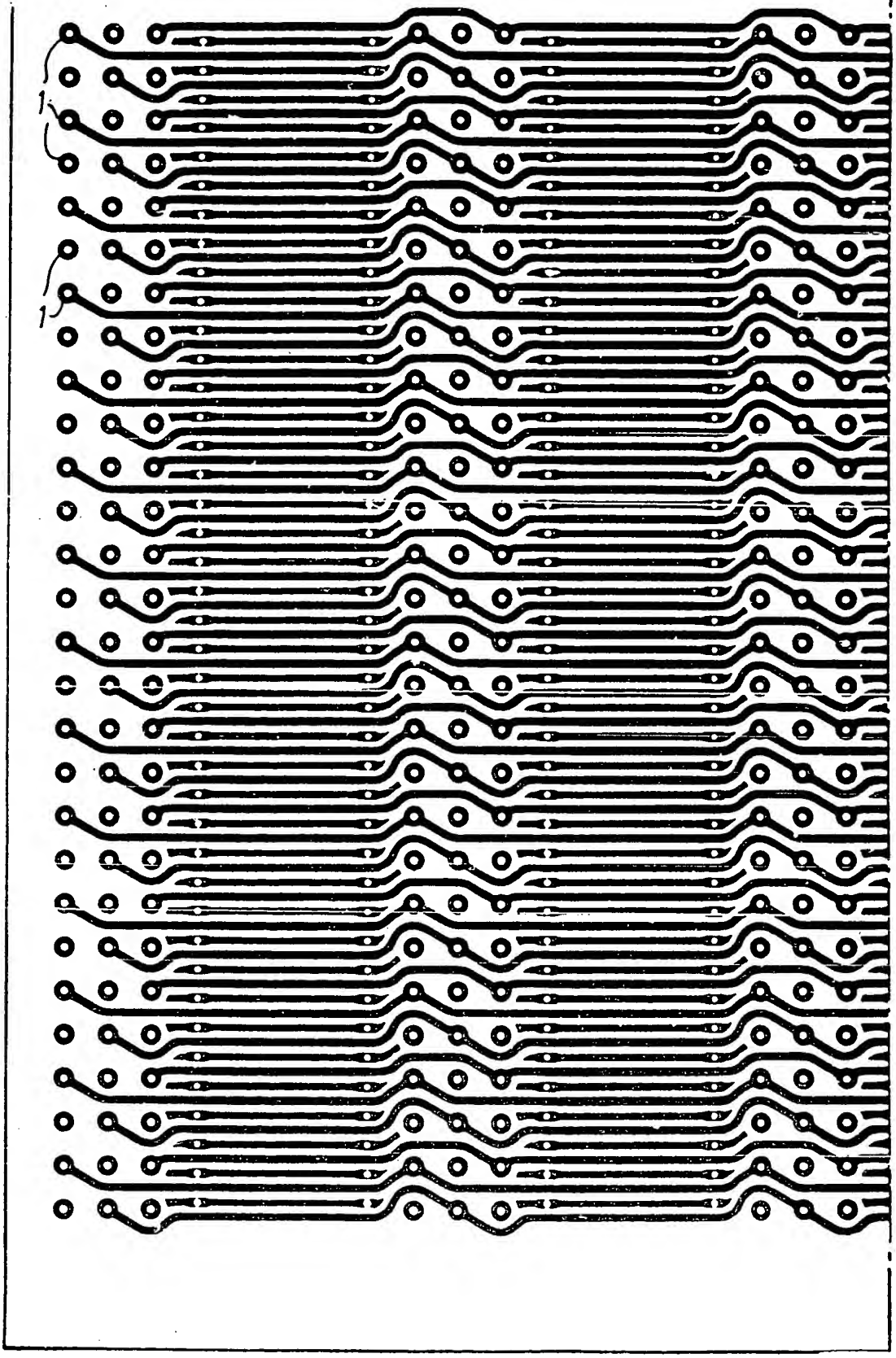
FIG. 3



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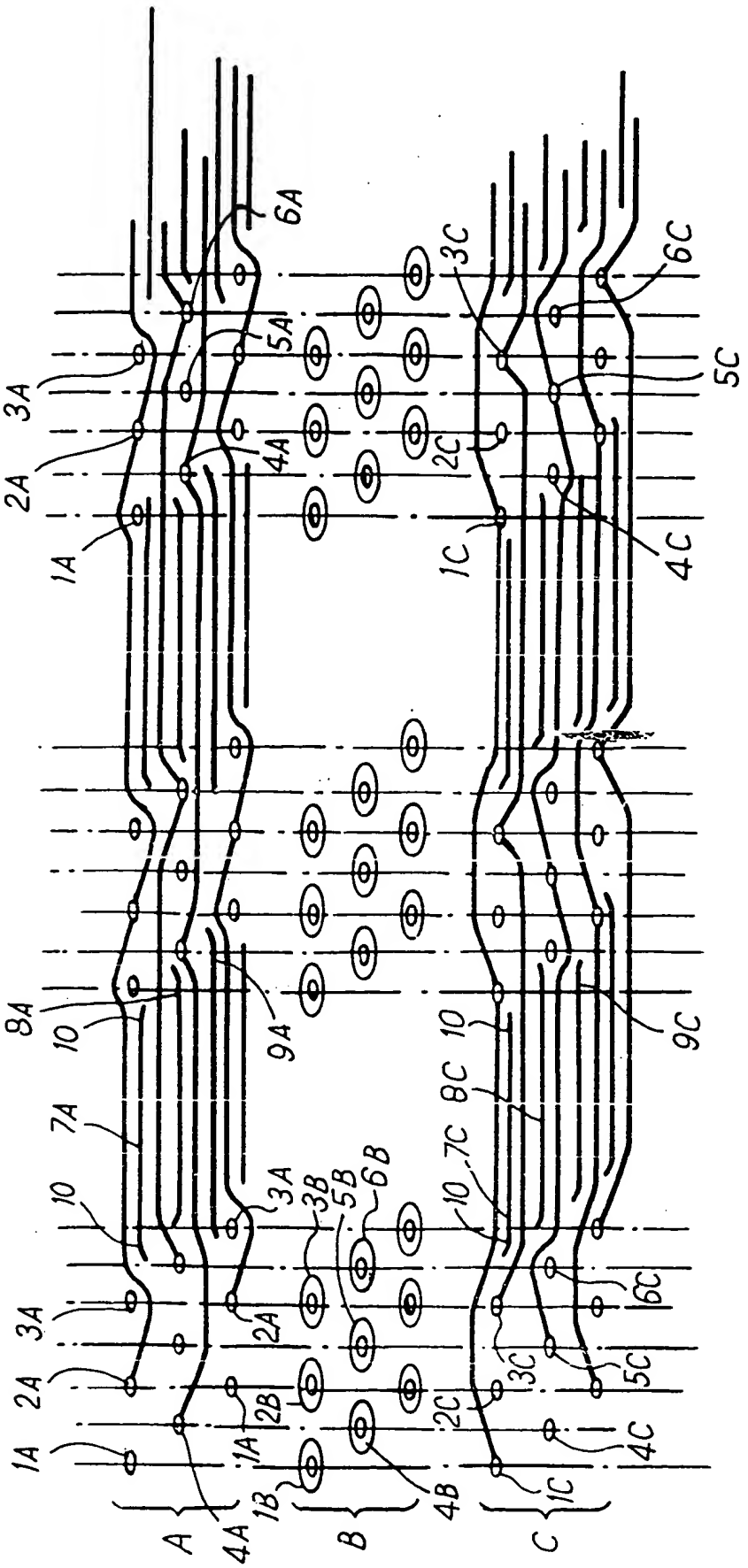

FIG. 4